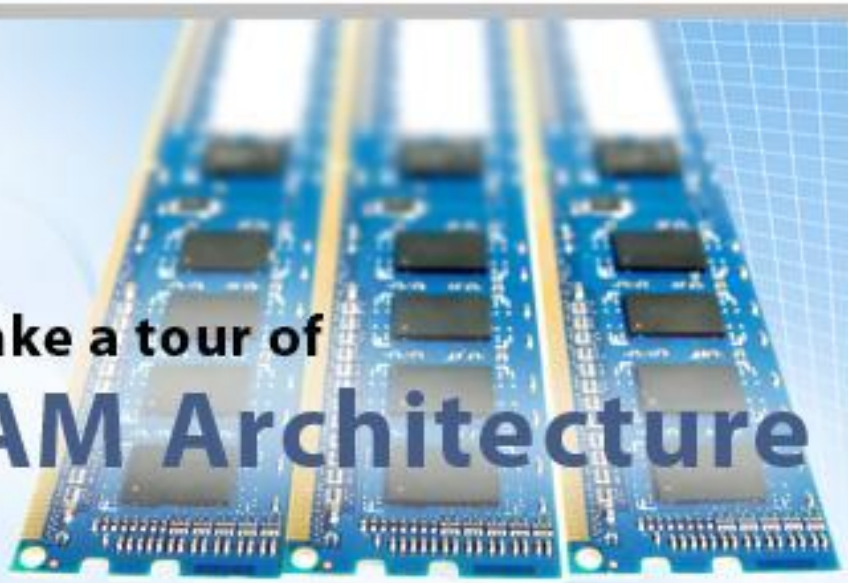
WIZLOGIX Pte Ltd



Built for the future – take a tour of

Modern DRAM Architecture

Let Wizlogix guide you through the DRAM memory technology of tomorrow. Our latest two-day course, brought to you by Mindshare, reveals the most modern, advanced and powerful computer memory system around, providing you with in-depth knowledge of DRAM architecture and design. You will take away a deep understanding of ultra-dense, high-speed DDR2/DDR3 technology as well as practical experience about how to design a DRAM memory channel on a system board.

A journey of discovery...

Everything you need to know about DRAM systems will be covered during this innovative course, from DIMM organisation and raw card definitions through to bus implementations and system design challenges. A place on our Modern DRAM Architecture course will literally transport your knowledge from basic to advanced in just a couple of days.

In this Modern DRAM Architecture course, you will learn:

- How a DRAM cell is organised
- Organisation of a variety of memory modules
- How to read DRAM transaction waveforms so that you can debug a memory channel
- Electrical characteristics of DDR2/DDR3 signals
- Elements of DRAM controller design
- How to design a DRAM memory channel on a system board

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About Wizlogix

Get on board today!

Duration: Two full days.
9.00 am to 5.30 pm

Location: Singapore

Register Now!

Contact us for more Information

Upcoming Courses
PCIe 3.0 Course
Register Now!

Certification for Instructors (IPC-CIT) and Specialists (IPC-CIS)

Course Length: 2 Days

Dr. Eric Bogatin - Power Delivery Network ▶

USB 3.0 SuperSpeed ▶

Who Should Attend?

Although this in-depth course is hardware centric, it is suitable for both hardware engineers and software/firmware engineers. It is an ideal learning forum for DRAM controller designers, chipset designers, system board-level designers and validation engineers.

Recommended Prerequisites

A basic understanding of memory architecture.

Course Material

Hard and soft copy of the Modern DRAM Architecture course presentation.

Attendees will be also be presented with a Certificate of Participation.

Course Outline

Day 1:

- **DRAM Introduction**
- **DRAM Chip Overview**
- **DRAM Module Overview**
- **SMBus Protocol and SPD EEPROM**
- **SDRAM Overview**
- **DDR1 Overview**
- **DDR2**
  - What has changed from DDR1?
  - SSTL_18 defined
  - Burst mode of 4 and 8 only (4 N prefetch)
  - ODT including timings
  - OCD (not used)
  - Posted CAS AKA additive latency
  - And command definitions
- **DDR3**
  - Fly-by-routing read example
  - Read calibration
  - Fly-by-routing write example
  - Write levelling
  - On-die termination
  - ZQ calibration
  - Reset
  - Package mirroring
  - Mode register changes

Day 2:

- **System Design Challenges**
  - Board layout topics
  - System architecture topics
- **Dram Controller Implementation**
  - Block diagram
  - Description of each functional unit
  - Path to FSB and path IO
  - Buffering/Combining unit (read and write paths)
  - Refresh timing control
  - Analog calibration unit
  - IO pad control unit
  - Physical address conversion
  - Control registers
- **Overview of Other Memory Types**
  - RL DRAM
  - GDDR
  - RAMBUS DRAMS
  - FBDRAM

Course Facilitator

Ravi Budruk is Senior Staff Engineer and Instructor at MindShare, Inc in the United States. He has 20 years of industry experience and has trained thousands of hardware and software engineers in various subjects of computer architecture. He is an industry expert on topics such as Intel x86 Processor Architecture, bus architectures such as Intel QuickPath Interconnect, HyperTran`sport, PCI Express/PCI/PCI-X, IEEE 1394, ISA, PC system architecture and a variety of memory (DDR2/DDR3) technologies.

Ravi is an excellent presenter and a dynamic speaker who brings industry-acquired experience to the class. He is author of the 'PCI Express System Architecture' textbook and is currently authoring a book titled 'Modern DRAM Architecture'.

Before joining MindShare, Ravi was an Intel processor-based chipset design engineer, a system architect and a manager at VLSI Technology, Inc. He has an MS degree in Electrical Engineering from Purdue University and a BS degree (Magna Cum Laude) in Electrical Engineering from Texas Tech University.

MindShare is the preferred training provider for an extensive list of clients that include:

ADAPTEC • AGILENT TECHNOLOGIES • ALCATEL-LUCENT • AMD • APPLE • BROADCOM • CADENCE • CISCO • CRAY • DELL • EMC • FREESCALE • GENERAL DYNAMICS • HP • INFINEON • IBM • KODAK • LSI • LOGIC • MARVELL • MICROSOFT • MOTOROLA • NASA • NATIONAL SEMICONDUCTOR • NETAPP • NOKIA • NVIDIA • PLX TECHNOLOGY • QLOGIC • QUALCOMM • SANDISK • SIEMENS • SUN MICROSYSTEMS • SYNOPSYS • TI • UNISYS • XEROX

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