

Get on board the next generation **PCI Express 3.0**

If you're not already familiar with PCI Express 2.0, it's time to take the fast track to update your knowledge.

The PCI Express (PCIe) architecture is a third-generation, high performance I/O bus used to interconnect peripheral devices in computing and communications platforms. PCI Express has been designed into consumer and high-end PCs, embedded computing, and communication markets and has established itself as the bus of choice for on-board I/O connections. This architecture is governed and defined by the PCISIG (Peripheral Component Interconnect Special Interest Group). MindShare's PCI Express System Architecture course starts with a high-level view of the design to provide the big-picture context and then drills down into the details for each part of the design, providing a thorough understanding of the hardware and software protocols. This course covers Gen1, Gen2 and Gen3 PCI Express.

Express Learning with Wizlogix

Sign up for our four-day PCI Express System Architecture course, brought to you by MindShare, Inc. and you will gain a deep understanding of PCI Express, how it works, what it can do and why it's the bus of choice for on-board I/O connections. Starting with a high-level view of the design, the course then drills down to the fundamentals of each part of the design. By course completion, you will have taken a direct route to a thorough understanding of both hardware and software protocols.

What You Will Learn

- How PCIe is backward-compatible with PCI and PCI-X
- The definition and responsibilities of each of the layers in the interface
- How the hardware-based automatic error detection and correction mechanism works
- The details of the packet-based protocol used by PCIe
- The address space and packet-routing methods used
- Differences between Gen1, Gen2 and Gen3
- The details of the configuration registers that provide control and status visibility to software



About Wizlogix

Course Details

Duration: Four full days,
9.00am to 5.30pm

Location: Singapore

Register Now!

Contact us for
more information



Upcoming Courses

USB 3.1 Course
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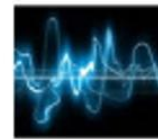


**Certification for
Instructors
(IPC-CIT) and
Specialist (IPC-CIS)**



**Dr. Eric Bogatin -
Power Delivery
Network**

Course Length: **4** Days



PCB Signal Integrity
& EMI Training ▶
(Lab Session Using
Allegro SI)

Who Should Attend?

- This Wizlogix course is hardware-oriented but is suitable for hardware, software or firmware engineers because the configuration registers used to control the hardware are covered in detail.
- The course is ideal for RTL-, chip-, system or system board-level design engineers who need a broad understanding of PCI Express.
- Because the course contains practical examples of transactions on the various bus interfaces, the course is also suitable for chip-level and board-level validation engineers.

Course Outline

- ❖ PCI Architecture Background Foundation
- ❖ PCI Express Features and Architecture Overview
- ❖ Configuration Overview
- ❖ Address Space and Transaction Routing
- ❖ TLP Format Overview
- ❖ Quality of Service and Arbitration Overview
- ❖ Flow Control Overview
- ❖ Transaction Ordering
- ❖ DLLP Format Details Overview
- ❖ ACK/NAK Protocol
- ❖ Physical Layer Logic (Gen1/Gen2) Fundamentals
- ❖ Physical Layer Logic (Gen3)
- ❖ Physical Layer Electrical (Gen1/Gen2/Gen3) Overview Only
- ❖ Link Initialization & Link Training
- ❖ Error Detection and Handling
- ❖ Power Management
- ❖ Interrupt Support
- ❖ System Resets

Recommended Prerequisites

A basic understanding of digital bus architectures such as PCI is highly recommended.

Course Material

MindShare will supply:

- 1) PCI Express Technology eBook by Mike Jackson and Ravi Budruk
- 2) Downloadable PDF version of the presentation slides

Course Facilitator



Ravi Budruk is a Senior Staff Engineer and Instructor with MindShare, Inc in the United States. He has 20 years of industry experience and has trained thousands of hardware and software engineers in various subjects of computer architecture. He is an industry expert on topics such as Intel x86 Processor Architecture, bus architectures such as Intel QuickPath Interconnect, HyperTransport, PCI Express / PCI / PCI-X, IEEE 1394, ISA, PC system architecture and a variety of memory (DDR2/DDR3) technologies.

Ravi is an excellent presenter and a dynamic speaker who brings industry acquired experience to the class. He is author of the 'PCI Express System Architecture' textbook and is currently authoring a book titled 'Modern DRAM Architecture'.

Before joining MindShare, Ravi was an Intel processor-based chipset design engineer, system architect and manager at VLSI Technology, Inc. He has an MS degree in Electrical Engineering from Purdue University and a BS degree (Magna Cum Laude) in Electrical Engineering from Texas Tech University.

MindShare is the preferred training provider for an extensive list of clients that include:

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