



# Experience acceleration – discover the USB 3.1 with xHCI



Each generation of the USB is backward compatible and a USB 3.1 topology may include devices operating at five speeds. USB 3.1 brings the 5th speed option, 10 Gb/s SuperSpeedPlus (SSP). The USB 2.0 and SS/SSP signals are physically separate and USB 3.1 refers to devices operating at LS/FS/HS as being in the USB 2.0 topology; devices operating at SS and SSP are in the Enhanced SuperSpeed (ESS) topology and are also referred to as ESS Gen1 and Gen2. In addition to the faster data rates, the ESS topology employs protocol optimizations including unicast packets, device asynchronous messages, as well as link level flow control, error handling, and power management.

All generations of USB rely on platform host controllers to manage devices attached to each bus instance. The advanced capabilities of USB 3.1 require a new generation of host controller. Course topics include Intel's eXtensible Host Controller Interface (xHCI). A single host controller based on xHCI can manage both USB 2.0 and Enhanced SuperSpeed topologies as well as attached devices of any USB speed. The xHCI operational model, software interface (registers, memory data structures), doorbell-based work notification, and hardware transaction scheduling are all described.



About Wizlogix

**Speed up your learning...read on to find out more**

**Duration:** Four full days, 9.00am to 5.30pm

**Location:** Singapore

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Contact us for more information

**Course Length: 4 Days**

## Who Should Attend?

This course is designed with hardware, software, and validation engineers in mind. Features and limitations of each generation of USB are described, as is the role of xHCI compliant host controllers in managing attached devices and hubs.

## Recommended Prerequisites

A background in USB 2.0 protocol is helpful.



### Upcoming Courses

PCIe 3.0 Course  
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Certification for Instructors (IPC-CIT) and Specialist (IPC-CIS)



Comprehensive Modern DRAM Architecture

# Course Material

Students will receive a copy of the USB 3.0 course presentation.

Attendees will also be presented with a Certificate of Participation.

## Grants Available

Email us for more information.



## Course Outline

### Part 1:

#### USB 3.1

- Introduction to USB 3.1
- ESS End-to-End Protocol
  - Role of the Host Controller
  - Introduction to Protocol Layer Packets
  - Gen 1 & Gen 2 IN/OUT Transactions

- USB 3.1 Hubs
- ESS Port-to-Port Protocol
- ESS Chip-to-Chip Protocol
- ESS Link Reset Events
- ESS Link Training
- Link Recovery and Retraining
- Enumeration and Configuration
- ESS Power Management

### Part 2:

#### eXtensible Host Controller Interface (xHCI) for USB

- Overview of xHCI
- xHCI Resources, Big Picture
- xHCI Internal Registers
- xHCI Memory Data Structures
- xHCI Interrupts
- xHCI Reset & Initialization
- Device Attachment & Initialization



## Course Facilitator



Jay Trodden is an electrical engineer and Instructor with MindShare, Inc. in the United States. He has 15 years of experience in electronic hardware design. As a MindShare instructor, Jay has trained thousands of hardware and software engineers on topics including Intel x86 Processors, chipsets, and bus protocols including PCI, PCI-X, PCI Express, AGP, HyperTransport, and USB 2.0/USB 3.0. He is an excellent teacher who brings insight and experience to the classroom. Jay is co-author of MindShare's HyperTransport System Architecture book and is currently working on a new book covering USB 3.0 and xHCI host controllers.

Jay has a BS degree in Electrical Engineering from University of Nevada and a BA degree in Education from San Francisco State University.

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