SIEMENS x WIZLOGIX Pte Ltd

SIEMENS EDA ASEAN WEBINAR SERIES

Where Today Meets Tomorrow

PARTICIPATE TO WIN!

Presented By: David Wiens
Product Manager

Date: 08 April 2021
Time: 10 am - 11am

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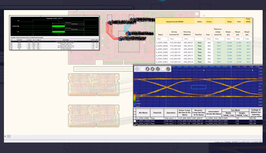
https://tinyurl.com/2ns4wbym

Managing Electronics Systems Design Risk with an Optimized Verification Strategy

Did you know that 58% of all projects incur additional costs or miss release deadlines? Discover how you can improve design quality by integrating verification throughout the design process by detecting problems earlier through best practice design automation to reduce risk of failure.



Ensuring DDR4 Electrical Performance at Intended Data-rate

Gather insights on how to optimize design margins in the post-layout simulation using the DDRx Wizard in Hyperlynx and understand how electrical considerations should be made during the post-layout verification process in this 1-hour webinar special.

Presented By: Min Maung
Senior Technical Marketing Engineer
Electronic Board Systems

Date: 06 May 2021
Time: 10 am - 11am

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https://tinyurl.com/tzbc2wam

Presented By: Don Kost
Technical Engineer

Date: 10 June 2021
Time: 10 am - 11am

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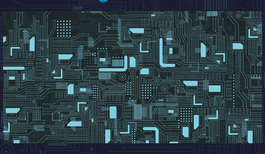
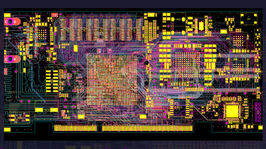


Optimize New Product Introductions Going Fast Right Or Both

Design for manufacturing (DFM) decisions place an important role in the yield, cost and reliability of your design. Learn how can DFM tools optimize your designs for manufacturing to facilitate better designs faster.



A Hybrid Design Verification Methodology for Increased Coverage and Faster Iterations

Automate tedious design inspections to identify common layout problems or detect hidden electrical issues that generate EMI or poor signal quality. Find out how a hybrid design verification methodology can solve your PCB layout issues.

Presented By: Rory Riggs
Technical Engineer

Date: 08 July 2021
Time: 10 am - 11am

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https://tinyurl.com/5ubky79z

Presented By: Min Maung / Todd Westerhoff
Product Manager

Date: 5 Aug 2021
Time: 10 am - 11am

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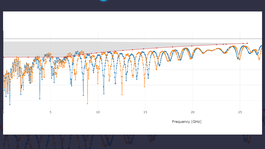

Designing SerDes Channels for Protocol Compliance

Master different types of SerDes channel compliance analysis using Channel Operating Margin and progressive analysis methods for efficient design processes. Build and validate accurate channel models to make good design decisions with Hyperlynx.

Error Reduction in the Design Definition Phase

Many engineers face issues such as pin voltage mismatch and wrong connections to voltage rails. Identify strategies to automate schematic analysis with Xpedition Valydate to overcome schematic design challenges and avoid minor issues that cause delays.

Presented By: Nicole Kyle
Technical Marketing Engineer

Date: 09 Sep 2021
Time: 10 am - 11am

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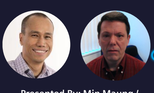
https://tinyurl.com/r47pxx8w



Presented By: Min Maung / Todd Westerhoff
Product Manager

Date: 30 Sep 2021
Time: 10 am - 11am

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https://tinyurl.com/tuyrn9f7

Automating Post-Route Verification for Multi-Gigabit Channels

Learn about different types of SerDes compliance analysis and how you can identify areas of a SerDes channel that require 3D EM modelling in the finale of the ASEAN webinar series.

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